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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

CHIOU-FENG CHEN ET AL.

Serial No. 10/753,103

Filed: January 6, 2004

For: NAND FLASH MEMORY WITH ENHANCED PROGRAM AND ERASE PERFORMANCE, AND FABRICATION PROCESS

Examiner: Johannes P. Mondt

Group Art Unit: 2826

Confirmation No. 2773

March 10, 2008

REPLY BRIEF

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Applicant responds as follows to the new points of argument made in the Examiner's Answer.

Claim 1

Bit Line Structure

As pointed out in applicant's Brief on Appeal, there are no bit lines, bit line contacts, or any overlapping or partial overlapping of a source region by a select gate. In his Answer, the Examiner has for the first time come forward with explanation for characterizing the drain region 124 of Hsu et al. as a bit line diffusion, and he has now taken the position that the bit line itself and the bit line contact are inherent so that the motivation he has failed to provide for combining selected features from the different references is not required.

Interestingly, in making that argument, the Examiner draws heavily upon a reference (Matas et al.) other than the ones upon which the rejection is based, and he mischaracterizes that reference providing evidence that "bit lines, bit line diffusion[s] and bit line contact[s] are inherent in a NAND Flash Memory cell array". While Matas et al. may show such elements in one figure (Figure 10-8), it certainly does not say that such elements are found in every NAND flash array or that they are inherent in such arrays.

What the Examiner is left with is an argument that it would be obvious to incorporate the bit line structure of Matas et al. or that shown in Figure 1 of applicant's drawings into the array shown in Hsu et al., but he has provided no motivation for doing so.

Select Gate Partially Overlapping Source Region

In arguing about the obviousness of incorporating the teachings of references such as Sakui et al. and Chapman et al. into the array of Hsu et al. in order have the last select gate in the row at least partially overlapping the source region, the Examiner overlooks the fact that the last select gate in the row (106d) is separated from the source region (126) by a memory cell (132d). Adding another select gate, which would serve no useful purpose in the array shown in Hsu et al., or removing the last memory cell and moving the source region over to the last select gate (106d) would be far beyond the teachings of the references.

Claims 15 and 19

In defending his rejection of Claim 15, the Examiner introduces a resourceful new definition of the term "directly above" as meaning that a vertical line can be drawn that

intersects the two bodies in question. That, of course, is contrary to the established meaning of the term, and it ignores the clear distinction made in applicant's specification and claims between a gate which partially overlaps a source region and a gate which is directly above a source region.

Claims 15 and 19 also distinguish over the references in the ways discussed above in connection with Claim 1.

Claim 24

Contrary to the Examiner's suggestion, the arrangement of stack gate structures perpendicular to the active region in the substrate does not provide a control gate and a floating gate with self-aligned sides. Moreover, the Examiner has misquoted Col. 5, lines 26+ of Hsu et al. as referring to "the setting of . . . stacked gates 'on the side and orthogonal to the active region 104'", when in fact what they actually say is:

> A plurality of control gates 120a - 120d are set on the substrate 100 and on the one side of the stack gate structures 106A - 106d respectively, and are orthogonal to the active region 104. Col. 5, lines 26 - 29.

Applicant trust that was an innocent mistake on the part of the Examiner and not a deliberate attempt to mislead the Board.

With regard to the Examiner's argument that the term "self-aligned" only introduces a limitation on the method of making the memory cell array, applicant would point out that even though the self-alignment is the result of the process by which the sides of the gates are formed, it is nevertheless a structural feature that cannot be ignored.

Dependent Claims

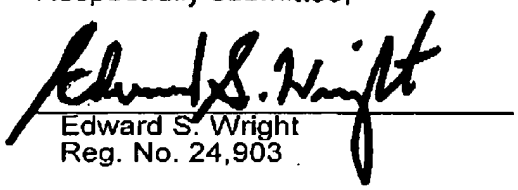
The remaining claims depend from Claims 1, 15, 19 and 24 and further distinguish over the references for the reasons discussed in applicant's Brief on Appeal.

With regard to Claim 2, however, applicant would point out that the Examiner has once again misquoted the teachings of Hsu, et al. as he did in connection with Claim 24.

SUMMARY AND CONCLUSION

It is once again respectfully submitted that the rejections which the Examiner has made cannot be sustained and that the action of the Examiner should be reversed.

Respectfully submitted,



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CERTIFICATE OF FACSIMILE TRANSMISSION

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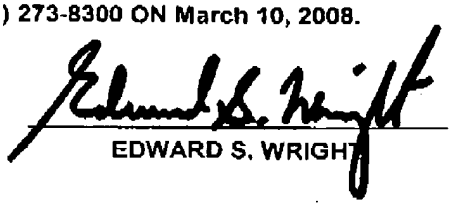

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